EXHIBIT N





(12) United States Patent Tomita et al.

US 6,320,819 B2 (10) Patent No.: (45) Date of Patent:

Nov. 20, 2001

SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

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both of Kawasaki (JP)

(73) Assignce: Fujitsu Limited, Kawasaki (JP)

Subject to any disclaimer, the term of this (*) Notice:

patent is extended or adjusted under 35

U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/733,961

Dec. 12, 2000 (22) Filed:

Related U.S. Application Data

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(30)	Fore	ign Application Priority Data	
Feb.	3, 1998	(JP)	10-022257

(51) Int. Cl. 7 G11C 8/00 365/194

365/230.08, 194

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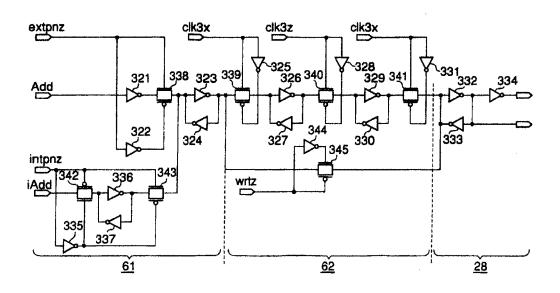
* cited by examiner

Primary Examiner-Huan Hoang (74) Attorney, Agent, or Firm-Arent Fox Kintner Plotkin & Kahn PLLC

(57)ABSTRACT

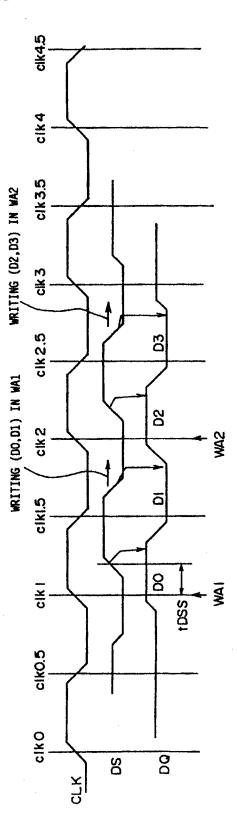
A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal includes address-latch circuits, a first control circuit which selects one of the address-latch circuits in sequence in response to the clock signal, and controls the selected one of the address-latch circuits to latch a corresponding one of the addresses in response to the clock signal, and a second control circuit which selects one of the address-latch circuits in sequence in response to the strobe signal, and controls the selected one of the address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

6 Claims, 25 Drawing Sheets



Nov. 20, 2001

Sheet 1 of 25

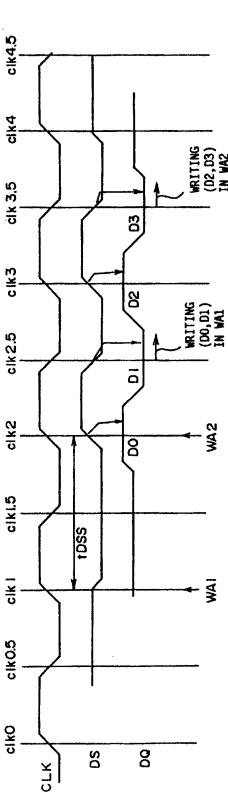


U.S. Patent

Nov. 20, 2001

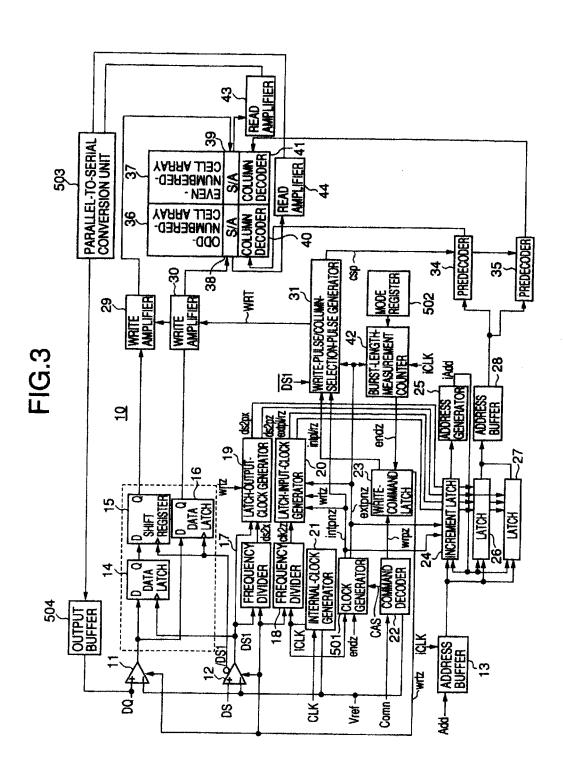
Sheet 2 of 25

US 6,320,819 B2



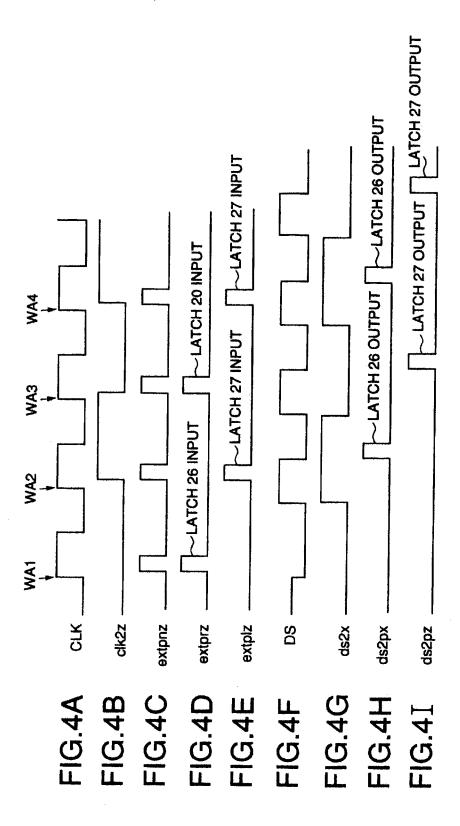
Nov. 20, 2001

Sheet 3 of 25



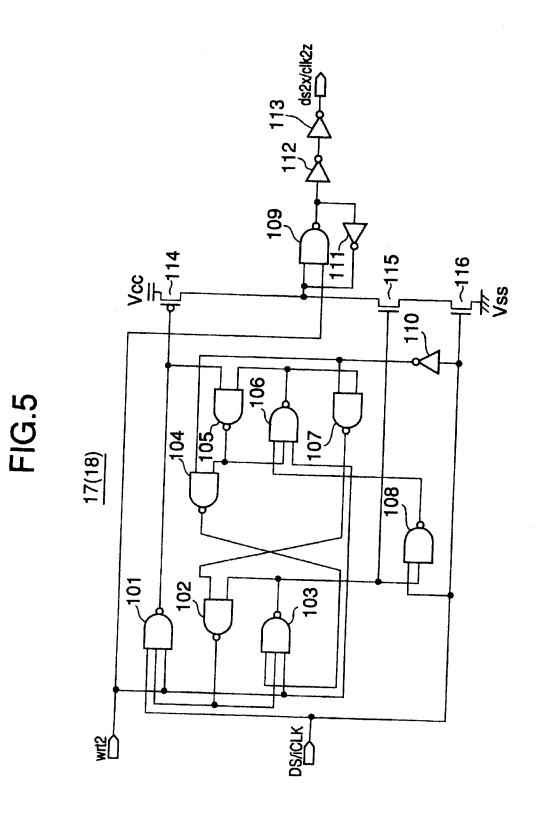
Nov. 20, 2001

Sheet 4 of 25



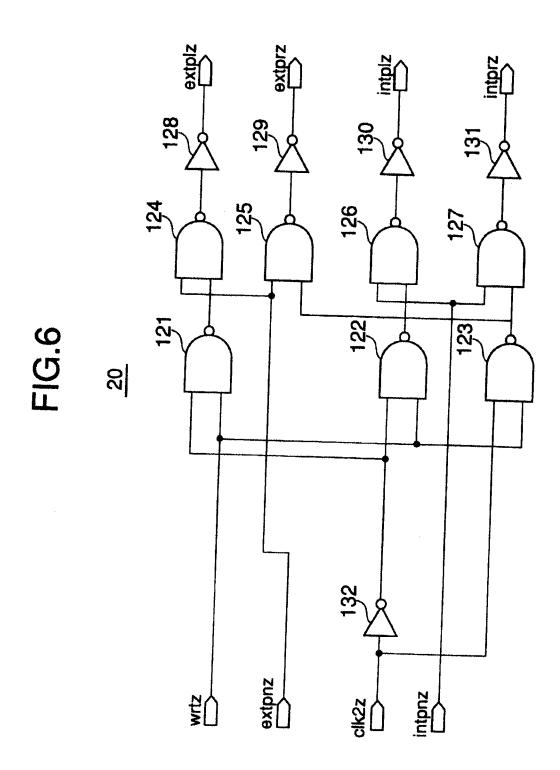
Nov. 20, 2001

Sheet 5 of 25



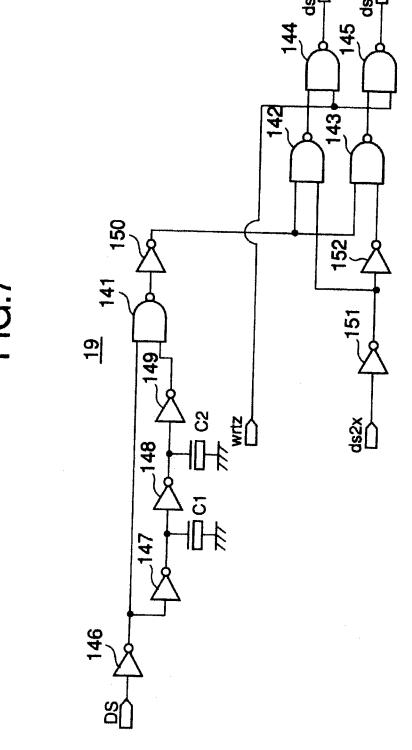
Nov. 20, 2001

Sheet 6 of 25



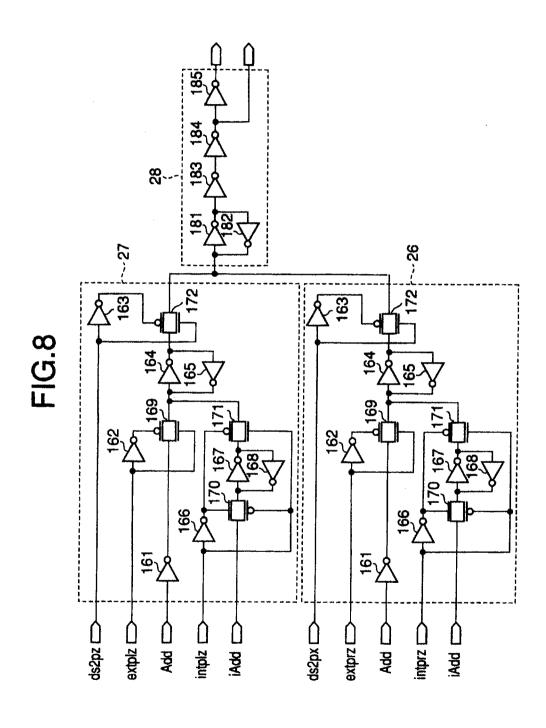
Nov. 20, 2001

Sheet 7 of 25



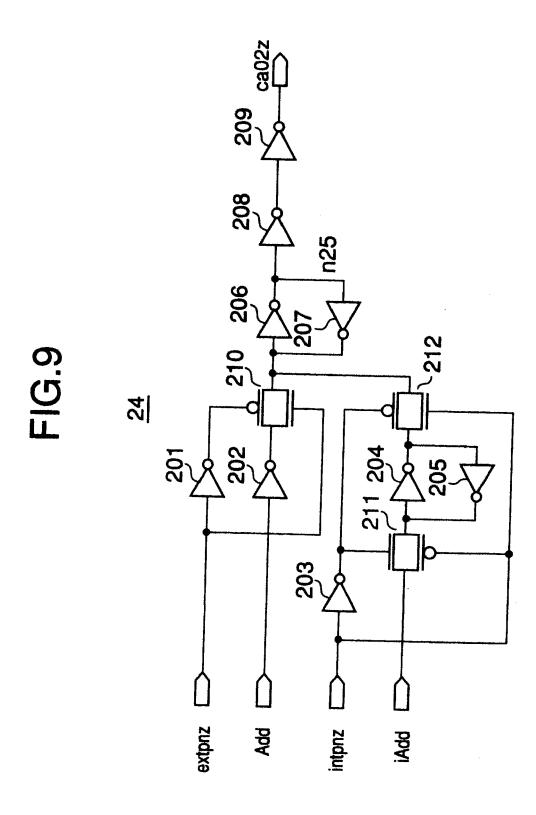
Nov. 20, 2001

Sheet 8 of 25



Nov. 20, 2001

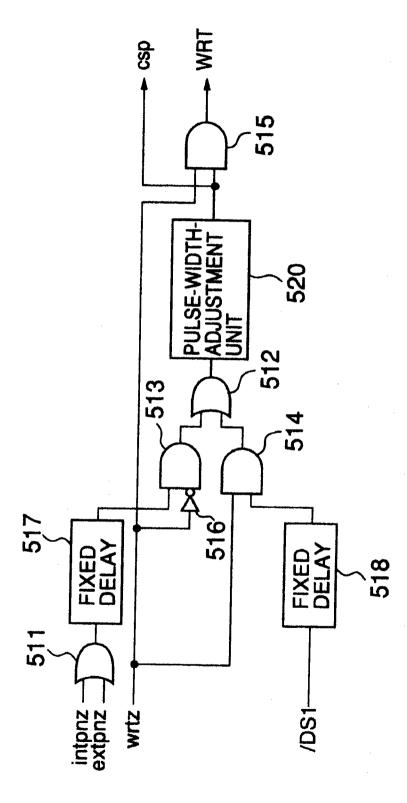
Sheet 9 of 25



Nov. 20, 2001

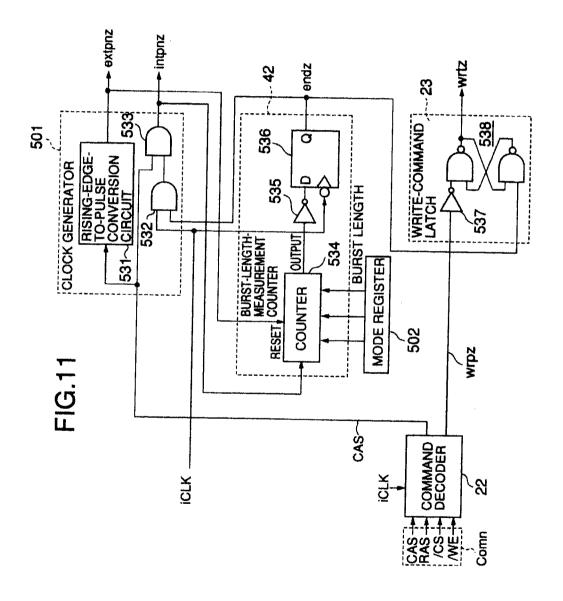
Sheet 10 of 25

FIG.10



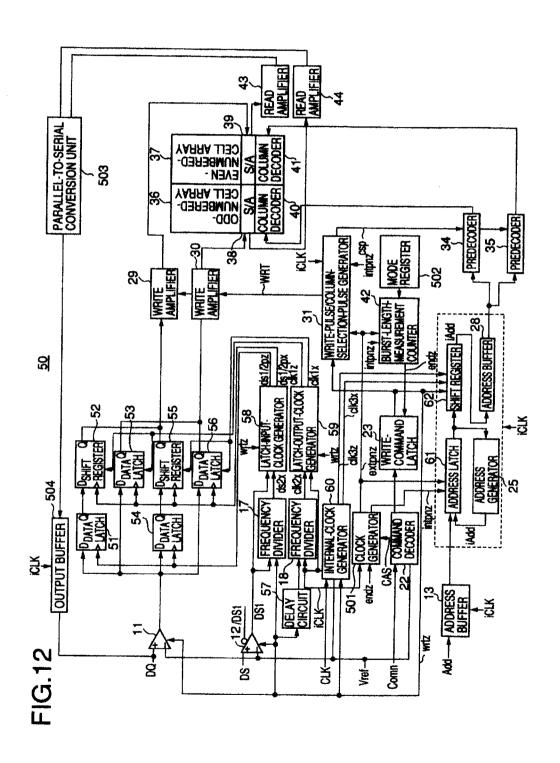
Nov. 20, 2001

Sheet 11 of 25



Nov. 20, 2001

Sheet 12 of 25



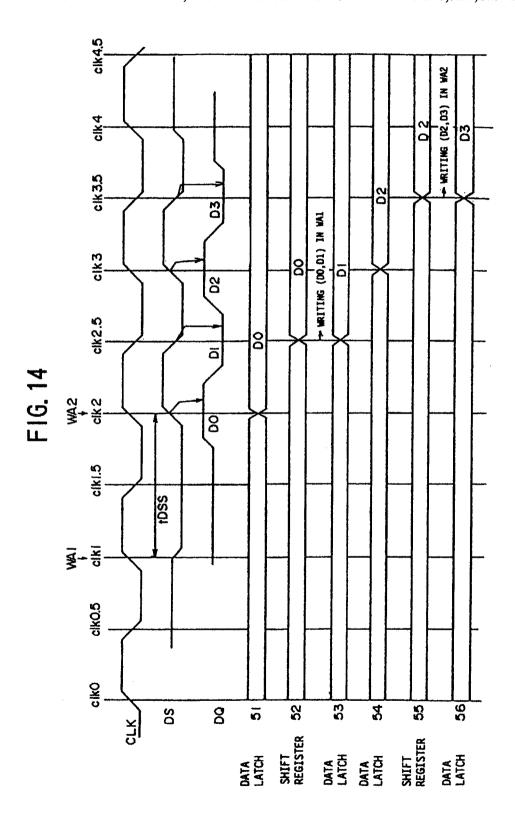
U.S. Patent Nov. 20, 2001 US 6,320,819 B2 **Sheet 13 of 25** WRITING (D2,D3) IN WA2 clk 3.5 -WRITING (DO, DI) IN WAI 20 8 8 8 ≅~≅ ross ciko.5 ciko SHIFT
REGISTER 52
DATA
LATCH
53 8 SO DATA

U.S. Patent

Nov. 20, 2001

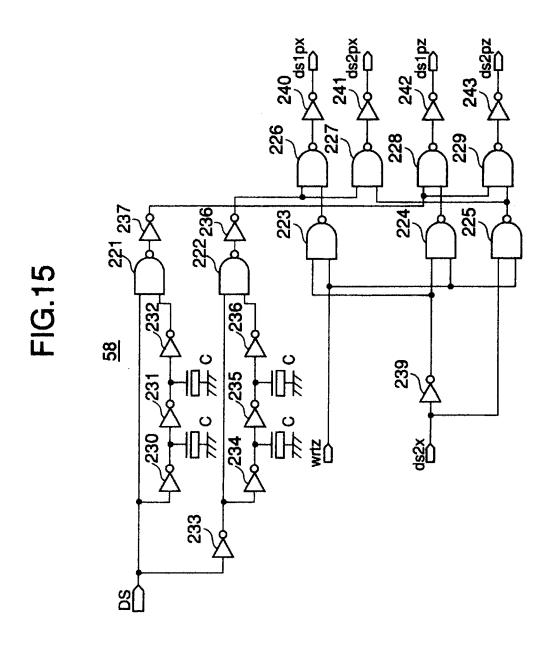
Sheet 14 of 25

US 6,320,819 B2



Nov. 20, 2001

Sheet 15 of 25



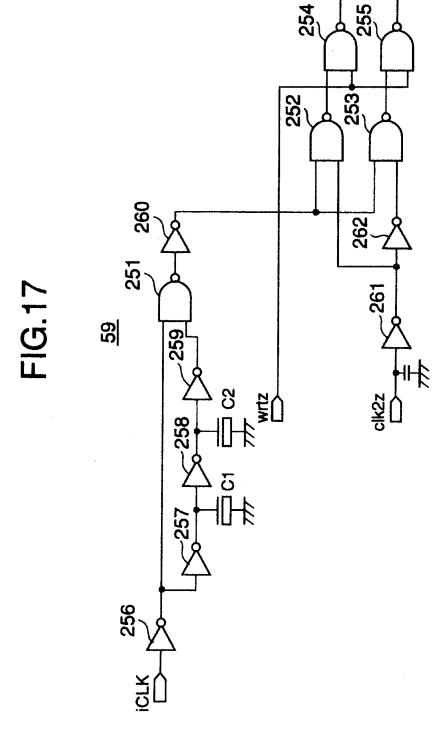
Nov. 20, 2001

Sheet 16 of 25

547 28 FIG.16 545 541 FREQUENCY DIVIDER DSI

Nov. 20, 2001

Sheet 17 of 25



Nov. 20, 2001

Sheet 18 of 25

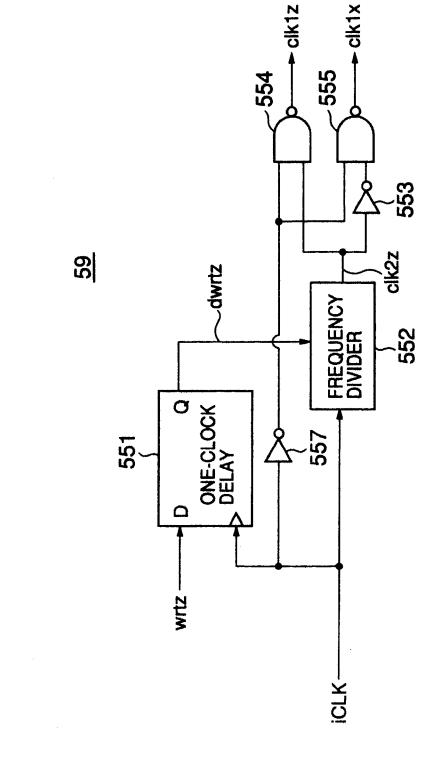


FIG.18